



domino (combinational OR combinatorial) stati

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Timing verification of sequential domino circuits - group of 13 »

D Van Campenhout, T Mudge, KA Sakallah - International Conference on Computer-Aided Design, 1996 - doi.ieeeecomputersociety.org

... are based on the SMO model for **static timing** analysis of ... step that computes the **combinational** delays ... A postprocessing step checks the **domino**-specific constraints ...
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... to gate level model extractor for simulation, automatic test pattern generation and verification - group of 2 »

S Kundu - Test Conference, 1998. Proceedings. International, 1998 - ieeeexplore.ieee.org

... in the fol- lowing four broad categories: **Combinational static** circuits, DCVS circuits (**static** or dynamic), pass gate logic and dynamic **domino** logic ...
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Timing verification and optimization for the PowerPC processor family - group of 3 »

RE Mains, TA Mosher, L van Ginneken, RF Damiano - Computer Design: VLSI in Computers and Processors, 1994. ..., 1994 - ieeeexplore.ieee.org

... and Time Zone Changes **Static timing** analyzers characteristically ... slave clock, propagated through **combinatorial** logic, and ... a stream of dynamic **domino** logic is ...
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Timing-driven partitioning and timing optimization of mixed static-domino implementations - group of 5 »

M Zhao, SS Sapatnekar - Computer-Aided Design of Integrated Circuits and Systems, ..., 2000 - ieeeexplore.ieee.org

... that the input is a **combinational** logic network ... violate the **timing** constraints of **domino** logic. ... based on the **timing-driven static-domino** partitioning algorithm ...
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Citation - group of 2 »

D Van Campenhout, T Mudge, K Sakallah... - eecs.umich.edu

... are based on the SMO model for **static timing** analysis of ... step that computes the **combinational** delays ... A postprocessing step checks the **domino**-specific constraints ...
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Timing verification of sequential dynamic circuits - group of 7 »

D Van Campenhout, T Mudge, KA Sakallah - Computer-Aided Design of Integrated Circuits and Systems, ..., 1999 - ieeeexplore.ieee.org

... **domino** logic, a variant of **domino** logic. ... Mudge-Olukotun (SMO) model for **static timing** analysis of ... a preprocessing step that computes the **combinational** delays ...
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Slope propagation in static timing analysis - group of 10 »

D Blaauw, V Zolotov, S Sundareswaran - Computer-Aided Design of Integrated Circuits and Systems, ..., 2002 - ieeeexplore.ieee.org